

IN THE SPECIFICATION

Please amend the specification as follows:

Page 4, line 11 – page 5, line 5:

The modulating circuit 902 is configured so as to be operated by the single power supply VDD (for example, 10 V). Consequently, the low level of the pulse signal which is the output signal of the circuit is equal to the ground potential (0 V), and the high level is equal to the voltage (10 V) supplied from the power supply VDD. When the pulse signal having such signal levels is used as it is, ~~therefore~~, the power-MOS transistor 904 in which the drain is connected to a positive power supply VPP+ (for example, +50 V) cannot be sufficiently controlled to the on state because of the characteristics of a MOS transistor, and the power-MOS transistor 905 in which the source is connected to the negative power supply VPP- (for example, -50 V) cannot be sufficiently controlled to the off state. Therefore, the drive controlling circuit 903 must have a function of controlling the power-MOS transistors 904 and 905 on the basis of the pulse signal which is modulated in the modulating circuit 902.

Page 8, line 18 – page 9, line 1:

The invention has been conducted in view of the circumstances noted above. It is an object of the invention to provide a class D amplifier in which output power-MOS transistors can be driven and controlled without using special circuit techniques or electronic components, and the use of a high-breakdown voltage process can be suppressed to a minimum required level.

Page 9, lines 2-3:

In order to ~~solve~~ achieve the aforesaid object, the invention is characterized by having the following arrangement.

Page 12, lines 11-21:

Fig. 1 shows the configuration of a class D amplifier DAMP according to the embodiment. Referring to the figure, a signal source SIG is a source of a (analog) music signal in which the midpoint of the amplitude is set to the ground potential (0 V). The signal of the signal source SIG is supplied as a music signal VIN to an input terminal TI of the class D amplifier DAMP via an input capacitor CIN. The class D amplifier DAMP is a so-called PWM amplifier, and configured by an input stage 100, a modulating circuit 200, a drive controlling circuit 300, and n-type output power-MOS transistors 401 and 402 (~~output transistors~~).

Page 12, line 25 – page 13, line 19:

The input stage 100 is configured by an input resistor R1, a feedback resistor R2 (= R1), and an operational amplifier OP. One end of the input resistor R1 is connected to the inverting input (-) of the operational amplifier OP, and the other end of the resistor to an input terminal T1. [[A]]
The feedback resistor R2 is connected between the inverting input and the output of the operational amplifier OP. A reference voltage VREF is applied to the non-inverting input (+) of the operational amplifier OP. The reference voltage VREF is generated by, for example, resistance-dividing a voltage which is supplied from a standard power supply VDD, and set to one half of the voltage of the power supply VDD. In the embodiment, the voltage of the power supply VD is "+10 V", or a standard power supply voltage in the art. The modulating circuit 200 converts a music signal output from the preceding input stage 100 by ~~means of the~~ applying PWM modulation to a pulse signal (PWM signal). The drive controlling circuit 300 complementarily drives and controls the output power-MOS transistors 401 and 402. The drive controlling circuit 300 will be described in detail later.

Page 13, line 21 – page 14, line 16:

The output power-MOS transistor 401 is used for outputting a high level to an output terminal TO, and the drain and the source are connected to a positive power supply VPP+ (high power supply) and the output terminal TO, respectively. The other output power-MOS transistor 402 is used for outputting a low level to the output terminal TO, and the drain and the source are connected to the output terminal TO and a negative power supply VPP- (low power supply), respectively. In the embodiment, the voltage of the positive power supply VPP+ is "+50 V", and that of the negative power supply VPP- is "-50 V". One of the input terminals of a loudspeaker SPK is connected to the output terminal TO via a low-pass filter consisting of an inductor L and a capacitor C, and the other input terminal of the loudspeaker SPK is grounded. The constant of the low-pass filter consisting of the inductor L and the capacitor C is set so that the carrier frequency component is removed away from the pulse signal which is output from the class D amplifier DAMP via the output terminal TO, and music signal components are passed through the filter.

Page 29, lines 1-15:

At this time, the internal circuit of the driving circuit 304 is supplied with the voltage VD1 based on the source voltage VS from the internal power supply P12, and hence the power supply system of the driving circuit 304 is raised with following the source voltage VS of the power-MOS transistor 401. ~~Therefore, also~~ In addition, the input threshold of the comparator CM1 is raised together with the source voltage VS. However, ~~also~~ the voltage VR1 generated by the biasing circuit P11 is raised with following the source voltage VS. Therefore, the levels of the signals H3 and H4 maintain the state conforming to the input characteristics of the comparator CM1 constituting the driving circuit 304, and the power-MOS transistor 401 is kept to the on

state. Under this state, the level of the signal H5 is higher than the positive power supply V_{PP+} by the voltage VD1 (= VDD).

Page 31, line 9 – page 32, line 1:

When the PWM signal is transferred at time t1 to the low level and the pnp bipolar transistors T3021 and T3022 are set respectively to the off state and the on state[.] ~~In response to this change,~~ the currents I5 and I6 flow in directions opposite to those in a period before the time t1, and the level relationship between the signals L3 and ~~[[L3]]~~ L4 is inverted. Consequently, the signal L5 output from the driving circuit 305 which receives the signals is changed to the high level. As a result, the gate voltage of the power-MOS transistor 402 becomes higher than the source voltage by the voltage VD2, and the power-MOS transistor 402 is set to the on state.

When the power-MOS transistor 402 is set to the on state, the source voltage VS of the power-MOS transistor 401 is lowered in accordance with the output signal OUT, and also the voltage VD1 which is generated by the internal power supply P12 based on the voltage is lowered.

Page 32, line 24 – page 33, line 9:

When the PWM signal is returned at time t3 to the high level, the signal H3 becomes the high level, and the signal H4 becomes the low level at time t4 in response to this transfer. Therefore, the driving circuit 304 which receives the signals H3 and H4 outputs the high level as the signal H5, and the power-MOS transistor 401 is set to the on state. In the low-side driver, the signal L3 becomes the low level, and the signal L4 becomes the high level. Therefore, the driving circuit 305 which receives the signals L3 and L4 outputs the low level as the signal L5, and the power-MOS transistor 402 is set to the off state.

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